REMARKS

In the specification, paragraphs [0015] and [0028] have been amended to mention new Figure 9.

New Figure 9 has been added to illustrate a delay circuit added to an output terminal of an off-chip driver. Support for new Figure 9 can be found throughout the specification, and in particular in paragraphs [0010], [0032], [0038], and original claim 3.

Claims 1-3, 6 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Watkins et al. (US Pat. 6,359,483). As a technical matter, applicant believes that Watkins is a 102(a) reference and that claims 1-3, 6 and 7 should have been rejected under 35 U.S.C. 102(a). Claims 5 and 10-15 are new and are fully supported by the specification. Claims 1-4, 8 and 9 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicants have amended dependent claims 1-4, 8 and 9. The Examiner's rejections under 35 U.S.C. § 112, second paragraph, are now moot.

The Examiner asserts that the cited reference discloses off-chip drivers (NAND gate 144-156), delay circuit (128-140), a pre-driver circuit (NAND gate 142) and an output driver circuit (multiple input NAND gate). However, applicant respectfully traverse these allegations as follows:

The driver circuit of amended independent claim 1 includes, *inter alia*, "a plurality of delay circuits at least two of which have different delay times, in which the delay circuits receive a data signal and generate delayed data signals ..." This configuration is illustrated Fig. 2, wherein the delay circuits (110-1...110-N) of the embodiment of Fig. 2 are connected in parallel with respect to each other so that a data signal is input at the same time into a plurality of delay circuits. In contrast, Watkins discloses delay circuits (128-140) that are

AMENDMENTS TO THE DRAWINGS

Please add FIG. 9.

Attachment: New sheet

connected in series with respect to each other so that just one signal is input into a single delay circuit (128).

Independent claim 1, as amended, also includes "a plurality of delay circuits, at least two of which have different delay times..." This allows a plurality of data signals to be output with a time delay so that the data signals output from the off-chip driver circuit do not experience turn on/off at the same time at a high frequency state. Nowhere in Watkins does it disclose delay circuits having a different delay time with respect to each other. In fact, Watkins teaches away from the invention recited in claim 1 by advocating the use of all delay circuits with an equal time delay. Watkins teaches this configuration of a delay circuit for the purpose of controlling the delay time of a clock signal, not a data signal, for synchronization purposes.

Independent claim 1 also includes "a plurality of off-chip drivers" that operate at the same time and "wherein the number of the off-chip drivers to be activated is changed from 0 to N in response to the respective control signals." Thus, the number of off-chip drivers that are operated varies from 0 to N according to the control so that drivability can be adjusted. It is respectfully submitted that Watkins makes no such disclosure. Specifically, the off-chip drivers (114-156) disclosed in Watkins do not operate at the same time, because the circuit disclosed in Watkins is designed such that only one off-chip driver is operated by the control signal (shift register output signal).

As mentioned above, the invention recited in independent claim 1 is generally directed to a circuit to control drivability, such that data signals output from an off-chip driver circuit do not undergo turn on/off at the same time at a high frequency state by giving different delay times to the data signals input into the off-chip drivers. In contrast, Watkins generally discloses a circuit to control delay time of a clock signal for the purpose of

synchronization. Therefore, the circuit disclosed in Watkins is directed to completely unrelated subject matter as that of the claimed invention, and those of ordinary skill in the art would not have looked to Watkins to derive the structures found in amended claim 1.

Accordingly, Applicant believes that the claim 1, 3, 6 and 11, as well as the claims dependent thereon, are distinguishable from Watkins and in condition for allowance. In view of the above amendments and remarks, applicant believes the pending application is in condition for allowance, and respectfully requests that a timely Notice of Allowance be issued in this case..

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Respectfully submitted,

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